AN INTEGRATED ΔΣ A/D ARCHITECTURE FOR SMART ISFET

ARQUITECTURA INTEGRADA ΔΣ A/D PARA UN SMART ISFET

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In this paper, we present an architectural and electrical design of an integrated A/D converter configuration, based on ΔΣ modulation, for data acquisition from an ISFET (Ion Sensitive Field Effect Transistor) microsensor, applied to the development of a Smart ISFET. This A/D architecture in continuous-time, incorporates the microsensor as a component of the integrated circuit, together with the required electronics for the automatic correction of the ISFET's offset fulfilling the necessary requirements for the development of a portable device.

En este trabajo presentamos el diseño arquitectural y eléctrico de una configuración de conversor A/D integrada, basada en la modulación ΔΣ, para la adquisición de datos de un microsensor ISFET (Transistor de Efecto de Campo Sensible a Iones), aplicado al desarrollo de un Smart ISFET. Esta arquitectura A/D en tiempo continuo, incorpora al microsensor como componente del circuito integrado, así como la electrónica requerida para la corrección automática del offset del ISFET, lo cual permite dar cumplimiento a los requisitos necesarios para el desarrollo de un dispositivo portátil.

I. INTRODUCTION

The ISFET microsensors are, intrinsically, pH chemical sensors, but they can detect and quantify other ions and molecules when are modified with different inorganic and organic membranes, giving rise to devices such as the so-called Chemically Modified Field Effect Transistors (CHEMFETs) and Enzymatic Field Effect Transistors (EnFETs), among others [1].

In the early 1970s, for the first time, Bergvel reported ISFETs as a modification of the Field Effect Transistors of Metal-Oxide-Semiconductor Structure (MOSFETs) [2]. These microsensors, shown in figure 1, are very similar to MOSFETs, which make them ideal for their microelectronic integration. This similarity also provides advantages such as low noise level, low power consumption, and reduced size, useful properties for their application in the increasingly demanded portable devices. In addition, ISFET´s intrinsic characteristics (low output impedance, robustness, durability, short response time, low manufacturing cost), gives it advantages over other conventional sensors such as, for example, glass electrodes for pH measurement [3, 4]. They can be used in diverse applications in biomedical and environmental fields and in analytical chemistry among others areas [4, 5].

The most recent work related to ISFETs focus on achieving adequate instrumentation for applications potentially linked to the molecular environment, also making use of sensor arrays with their associated electronics in each pixel. In this sense, the works developed by the group of Dr. P. Georgiou from the Imperial College reported real-time detection of genetic material making use of typical polarization

configurations, based on the modified common source configuration [6]. Other studies reporting instrumentation associated with ISFETs focus on the pH-time conversion, and are more oriented to detection than to quantification. An example is the work carried out by Y. Jiang for the detection of the bacterium E. coli [7].
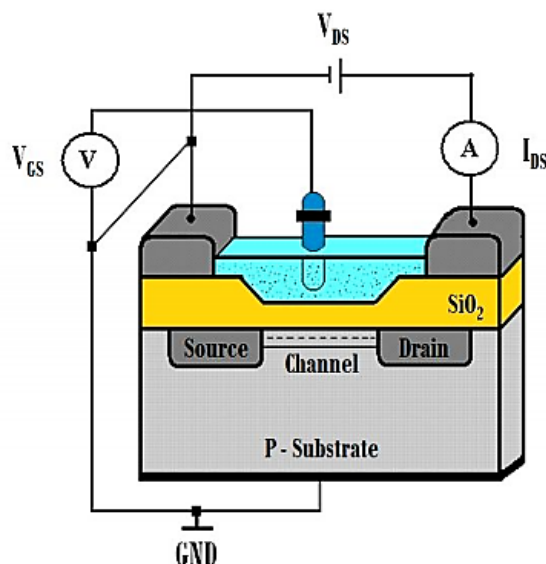

Figure 1. Schematic cross section of an N type ISFET.

Both lines of work have managed to reduce the offset and drifts of ISFETs, but not so much the noise associated with the instrumentation. In this work we present a new Smart ISFET model based on continuous-time (CT) and fully adjustable second-order ΔΣ A/D interface, which allows

the integration of an ISFET microsensor, with the requiring polarization elements for its operation, and its automatic electronic offset compensation, as well as the data acquisition and digitization stages. The architecture proposed in this work also has advantages such as a significant reduction in the number of components, compared with discrete electronics, low power consumption, low noise and auto-calibration of the microsensor, together with the attenuation of some of their limitations.

This new design will facilitate the development of portable devices for their applications in measurement of physiological chemical variables associated with certain diseases, for example, cystic fibrosis or an undesirable physiological state, such as dehydration. The work is organized as follows: Section II presents the Smart ISFET´s architecture and its characteristics; Section III, offers the electrical design at transistor level, with emphasis on the $\Delta\Sigma$ A/D; Section IV reports the simulation results and finally, Section V presents the conclusions.

II. SMART ISFET $\Delta\Sigma$ A/D ARCHITECTURAL DESIGN

Figure 2 presents the Smart ISFET's general scheme. The acquisition and digitization data coming from the microsensor are achieved with the use of a second-order continuous-time delta-sigma modulator ($\Delta\Sigma$M).
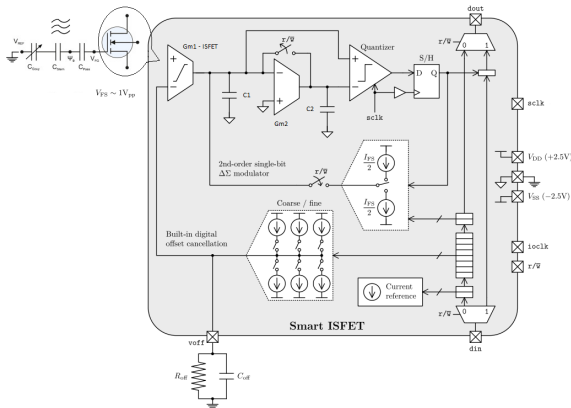

Figure 2. General scheme of Smart ISFET.

The general scheme is basically the architectural scheme of the designed ASIC. In the upper part of the figure are the main elements of the sigma-delta ADC (transconductance amplifiers $G_{mg1,2}$, the comparator and a D-type Flip Flop). In order to correct the ISFET offset, in the lower part of the figure we can see a current DAC with its input connected to a control logic and its output to the first transconductance amplifier (OTA).

The diagram also shows the input/output terminals. Among them, the input signal (V_{FS}), connected to the non-inverting terminal of the first OTA representing the gate voltage of the microsensor.

In the figure 2 we can also see the elements corresponding to the passive current filtering stage for cancellation of

accompanying current noise. In section III, we explain the main blocks of this scheme related to the Sigma-Delta modulator.

In figure 2, the input signal corresponding to the gate voltage of the ISFET (V_{FS}), and related to the ionic concentration in the active region of the microsensor, can operate in a range of 1 V_{P-P}, by design. This signal, along with the feedback signal, starts the A/D conversion cycle.

In comparison to more complex architectures the most outstanding features of this proposal are its excellent linearity/bit characteristic, its high resolution (with only 1 bit of quantification) and its simplicity for its microelectronic integration. Furthermore, its wide adjustment possibilities from different $\Delta\Sigma$ configurations, gives flexibility for the control of energy consumption and for its self-calibration and the system calibration.

Furthermore, among the most important quantitative features of this architecture are the oversampling ratio (OSR), the oversampling frequency (F_{OSR}) and the order of the modulator (n). All of these characteristics are related to the signal-to-noise ratio parameter (SNR), which, at the same time, has a close relationship with the resolution (B) of conversion [8, 9]. Equation 1 shows this relationship.

$$SNR = \frac{3\pi}{2} \cdot (2^B - 1)^2 \cdot (2n + 1) \cdot \left(\frac{OSR}{\pi}\right)^{2n+1} \quad (1)$$

Notice how an increase in the OSR or in the order of the modulator, generates an increase in the resolution of the A/D converter due to an increase in the SNR. This is an important issue to consider in the design stage.

Another important issue at this stage, in order to provide an output signal in each integrator according to the desired conversion resolution, is the determination of the integration constants G_{m1} and G_{m2}. With the aim to minimize the complexity of the design, it has been imposed that both transconductances values and therefore the integration constants be equal. These constants are calculated from the relationships expressed in equation 2 taking into account the frequency value obtained by the expression 3 for the frequency F_2.

$$F_{1,2} = \frac{1}{2\pi} \frac{G_{m1,2}}{C_{1,2}}, \quad (2)$$

$$F_2 < \frac{F_{OSR}}{2\pi}. \quad (3)$$

The frequency values $F_{1,2}$ were obtained for capacitance values of C_1 = 32 pF and C_2 = 8 pF, respectively. The $G_{m1,2}$ values were adjusted to get $F_{1,2}$ values of 0.5 kHz and 2 kHz, respectively to ensure a working resolution of the order of 12 bits, leaving an error margin of ±1 bit.

According to the previously calculated frequency values $F_{1,2}$, in figure 3 is shown the occupancy histogram for the output signal of the integrators. This graph shows the non-saturation of the integrators, since as it can be seen, the samples are not dispersed, but confined in a narrow voltage range between ±0.1 V.

The table 1 summarizes the main general design parameters, according to the requirements established for the system to implement.
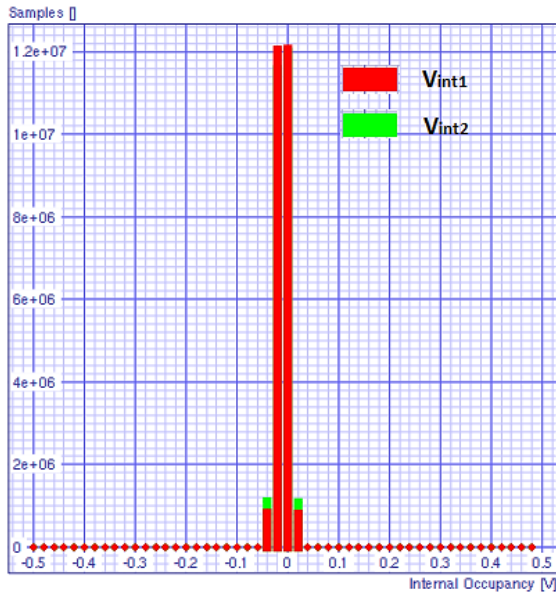

Figure 3. Occupancy histogram (integrator output response).

Table 1. Summary of the main parameters of the system

Signal frequency (F_{Signal})	62.5 Hz (Ω)
Sampling frequency (F_{OSR})	64 kHz
Oversampling ratio (OSR)	128
Bandwidth (BW)	250 Hz
Effective Number of bits (ENOB)	12 bits
Gain of integrators ($G_{m1} = G_{m2}$)	100 ns

III. ELECTRICAL DESIGN OF THE $\Delta\Sigma$ A/D ARCHITECTURE FOR THE SMART ISFET

In order to manufacture the Smart ISFET with CMOS technology of 2.5 microns (CNM25) it was necessary to design the necessary electrical blocks that make up the $\Delta\Sigma$ A/D architecture. By this way it was possible the integration of the ISFET microsensor, the electronics associated with its self-calibration, as well as the data acquisition and digitization stages.

III.1. Integrator with constant transconductance (G_m)

A step of great importance is the design of the transconductance values ($G_{m1,2}$). Especially, the G_{m1} transconductance taking into account its necessary linearity requirements to preserve the information of the microsensor output signal. Figure 4 shows the basic electrical architecture scheme of the transconductance selected according to this condition.

This design scheme responds to the topology known as classical cross-coupled differential core, with the transistors MI4 (microsensor ISFET) and MI7 operating in saturation

mode. Corresponding to figure 2, terminal V_1 receives the V_{FS} signal from the microsensor. This configuration ensures linearity in differential pair for a given voltage range [10,11].
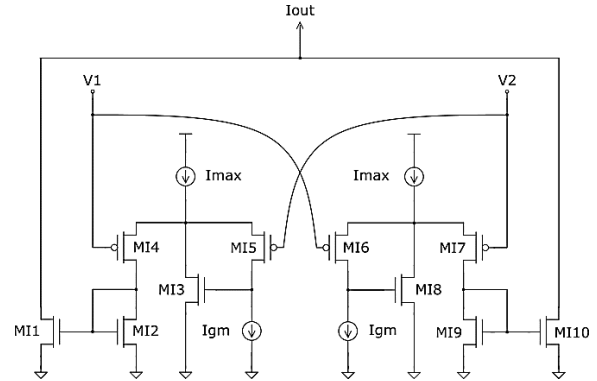

Figure 4. $G_{m1,2}$ - Electrical core design.

This condition is adjusted by the transistors MI3 and MI8, by maintaining a constant current flowing through the transistors MI5 and MI6. When the output current reaches ($+I_{MAX} - I_{GM}$) or ($-I_{MAX} + I_{GM}$), MI3 or MI8 are cut off. Above or below these current values the circuit shows a non-linear behavior as shows figure 5.
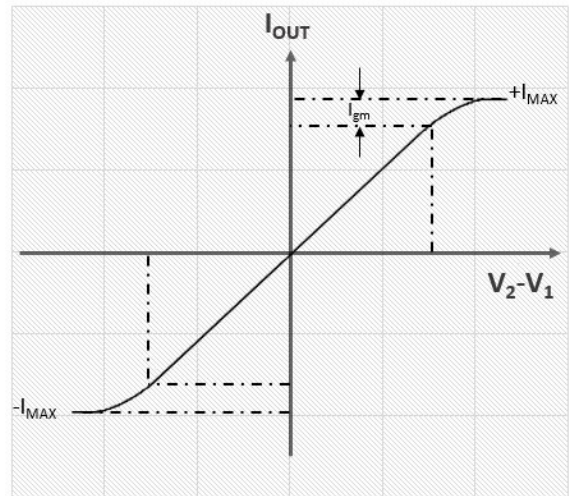

Figure 5. Limiting function for output current.

The resulting signal I_{out}, and its relationship to the adjustable transconductance, is expressed by equation 4.

$$G_m = \frac{I_{OUT}}{V_2 - V_1} = 2^2 \sqrt{\frac{2\beta I_{GM}}{n}} \tag{4}$$

III.2. Low power Latched Comparator

A latch-type comparator is an ideal option for the implementation of the 1-bit quantifier of a CT-$\Delta\Sigma$ A/D, due to its full output oscillation, high input impedance and absence of static energy consumption. Precisely because of this, an architecture based on this type of converter was designed [12,13].

Figure 6 shows the base architecture of the comparator designed.

This configuration, supplied with $I_{bias} = 1 \mu A$, mixes, with two inverters with preset in metastability, the currents that are generated in each branch of the differential input pairs (MI1, MI2) as a result of the voltage disparity in the terminals $+V_{IN}$ and $-V_{IN}$. The mix is controlled by a MI7 transistor in switch configuration and with a CLKZ control signal. By this architecture it is possible to significantly reduce the undesirable kickback input effect.

Furthermore, a D-type Flip Flop coupled to this architecture ensure an effective digitization of the signals (see figure 2).
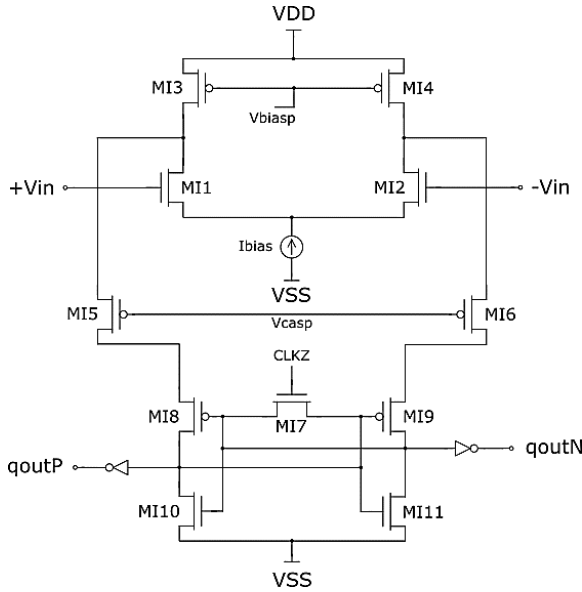

Figure 6. Latched comparator core.

The final digital signal is also part of the feedback of the ΔΣ modulator, that passes through a 1-bit current DAC, whose output signal is added to, or subtracted from the output of Gm_1, starting again an A/D conversion cycle.

The simulation tests performed to the comparator show values of 300 ns of conversion time, a power dissipation of 1.46 mW with a clock signal of 64 kHz.

IV. SIMULATION TEST PERFORMED

In order to evaluate the response of the system and its performance, a set of simulation tests were done using the free Spice Opus software, with the Spice 3 language.

The simulation tests are focused on three specific evaluations: signal-noise-distortion relation (SNDR), dynamic range (SQNDR) and occupancy histograms (integrator output response). These evaluations are crucial for the verification of the correct operation of the A/D converters [14].

IV.1. Signal-Noise-Distortion Ratio

As mentioned in Section II, the SNR is an important metric element when the dynamic behavior of an A/D converter is

evaluated. SNR is the relationship established between the output power at the frequency of a sinusoidal input signal and the bandwidth of the total quantization noise [15, 16]. Its relation to the resolution of the ΔΣ A/D converter was expressed by equation 1, but in terms of power. Equation 5 is used to calculate the SNR.

$$SNR(dB) = 10 \log_{10} \frac{P_{signalout}}{IBN}. \tag{5}$$

In this expression, $P_{signalout}$ is the output power at the frequency of an input sinusoid and IBN is the in-band quantization noise power.

The equation 5, accounts for the modulator linear performance only, so that the in-band power associated to harmonics of the input signal is not considered as part of the IBN to SNR computation. Therefore, it is important to obtain and evaluate the SNDR.

The SNDR is defined as the ratio of the output power to the frequency of an input sinusoid with respect to the total power of IBN (total), taking into account the possible harmonics at the output of the modulator ΔΣ. It is calculated similarly to the SNR [17].

Calculating the SNDR the distortions generated in the processed signal due to the non-idealities of the electronic components and circuits are taken into account resulting in a more detailed evaluation of the modulator performance.
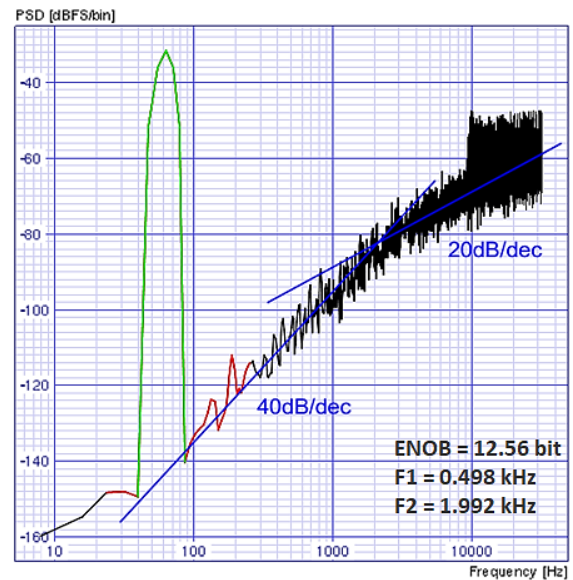
Figure 7 shows the corresponding graph to SNDR.

Figure 7. SNDR characteristics.

It can be seen that the maximum peak amplitude or maximum power, as expected, corresponds to the frequency of the analyzed signal and is set to 62.5 Hz. It can also see how the distortions are shifted outside of the bandwidth of the signal of interest. In addition, it can be seen that the slopes of the modulator noise distribution are 40 dB/dec, near the frequency band of the signal of interest and 20 dB/dec at the far end of it. These results confirm that, at the design level, we are in the presence of a second order system.

IV.2. Dynamic range

Dynamic range (DR) is another common performance metric for analog-to-digital converters (ADCs). DR describes the range of the input signal levels that can be reliably measured simultaneously, in particular the ability to accurately measure small signals, for which $SNR = 0$ dB, in the presence of the large signals [17]. It is calculated by means of equation (6).

$$DR(dB) = 10\log_{10}\frac{Y_{FS}^2}{2\cdot IBN}.\qquad(6)$$

Where Y_{FS}, is output sinusoid sweeping the full-scale range of the embedded quantizer, by a sinusoid with maximum amplitude at the modulator input.

In summary, the DR gives a notion of the ability of the A/D converter to detect and digitize small differences in amplitude between samples of a signal. This brings greater fidelity to the analogical signal from the microsensor.

Figure 8 presents the graph corresponding to the dynamic range.

This graph shows how the signal power increases, as the amplitude of the input signal increases, up to the maximum scale. This is in total correspondence with the typical behavior of the AD converter. In addition, the DR value, obtained at the x-axis intercept, is equal to -79 dBFS.
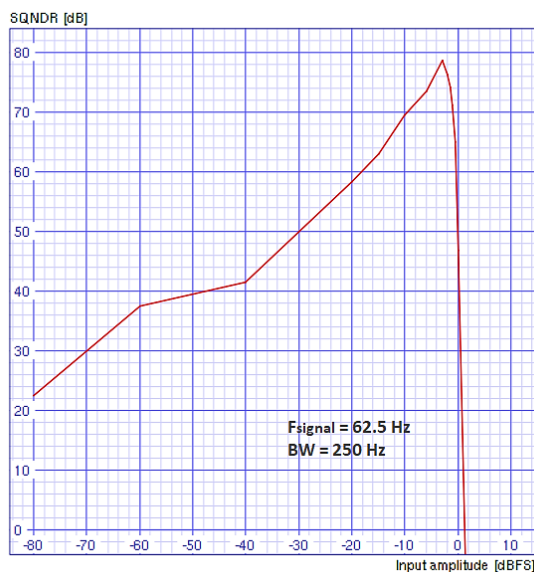

Figure 8. Dynamic range. Electrical scheme.

V. CONCLUSIONS

The work carried out demonstrates that it is possible to obtain a second-order, continuous-time and fully adjustable ΔΣ A/D converter architecture that, unlike other proposals, is less dependent on manufacturing technology and easier to implement at the microelectronic level. The new design integrates, in the same chip, an ISFET microsensor and the necessary elements for noise compensation and automatic correction of the microsensor offset, which offers advantages compared to other implemented designs. It is important to highlight that this architecture was designed in accordance with the requirements of portable technology, making possible to obtain an intelligent ISFET based on a robust, scalable, low cost and low energy consumption design, as the main core of a device capable to carry out non-invasive measurements of chemical variables in sweat samples, taking into account that, to date, no devices have been developed for this application.

The work carried out also lays the foundations for the future manufacture of this Smart ISFET (ASIC), in order to be able to practical validate the behavior of the device with real chemical measurements.

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